EDOS

HIGH RATE RETURN LINK PROTOTYPE BRIEFING

to the

EOSDIS TECHNOLOGY TRANSFER WORKSHOP

High Rate Return Link Prototype

Background - EDOS Prototyping

- EDOS HR prototyping efforts started in January 1995
- Purpose of prototyping was to reduce technical risk
  - achieving the 150 Mbps for the HRRL
  - HiPPI interface between HR Return Link Formatter Component (RLFC) and HR Service Processor
  - Mass Storage interface to the HRRL component
  - FDDI interface for file transfers

High Rate Return Link Prototype

Topics

- Summary of Prototype Results
- High Rate Prototype Within EDOS
- Functional Overview
- HRRL Service Processor Software Architecture
- Hardware Architecture
- HRRL Prototyping Results

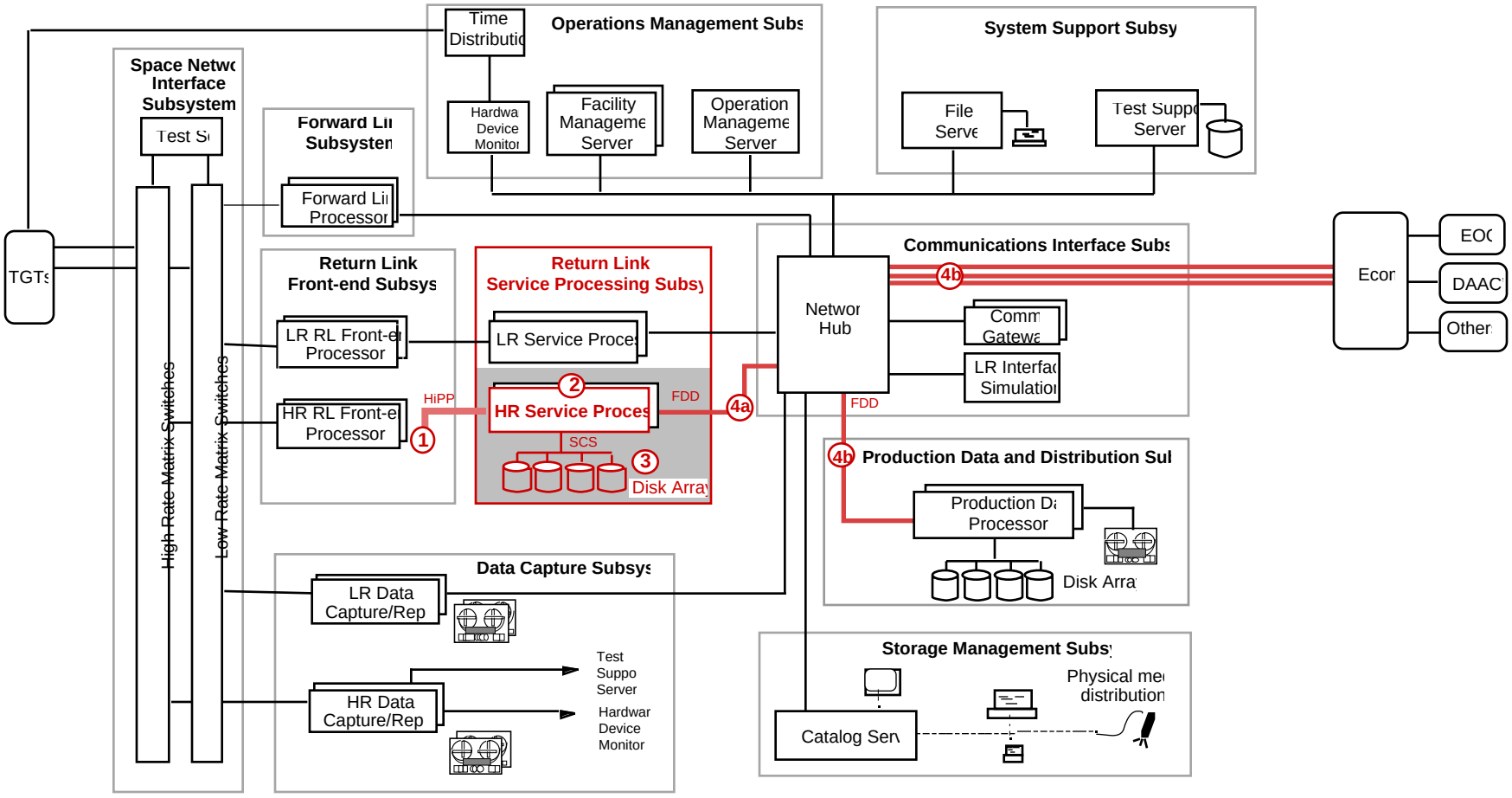
High Rate Return Link Prototype

Summary of Prototype Results

- **Our High Rate Return Link (HRRL) prototype software design and its implementation on a Symmetric Multiprocessor achieved (exceeded) the required EDOS HRRL rates**
  - **Virtual Channel Service: maximum achieved rate = 377 Mbps (150 Mbps required)**
  - **Path Service: maximum achieved rate = 172,000 - 206,000 pps (40,000 pps required) for 80 - 100 byte packets at ~150 Mbps**
  - **sustained runs exceeded 20 minutes (greater than a nominal TSS)**
- **Demonstrated the integration and performance of HiPPI and FDDI interfaces with the target platforms**
- **Achieved an efficient, integrated COTS Mass Storage solution**
- **Produced a reusable software solution for the EDOS HRRL development**
- **HRRL prototyping validates the EDOS design approach and minimizes technical risk**

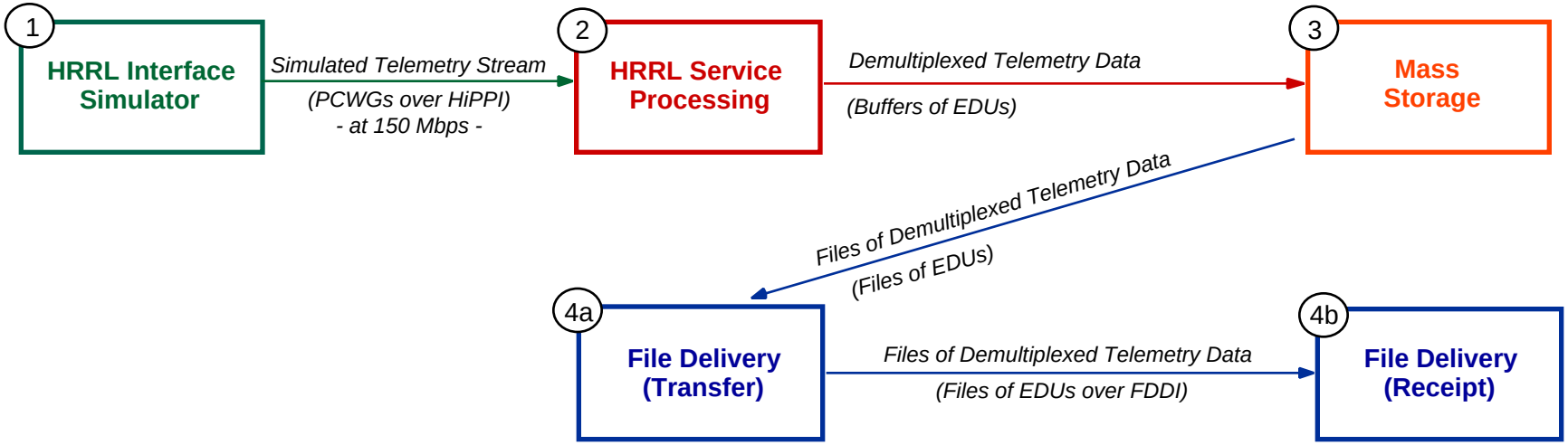
High Rate Return Link Prototype

High Rate Prototype Within EDOS

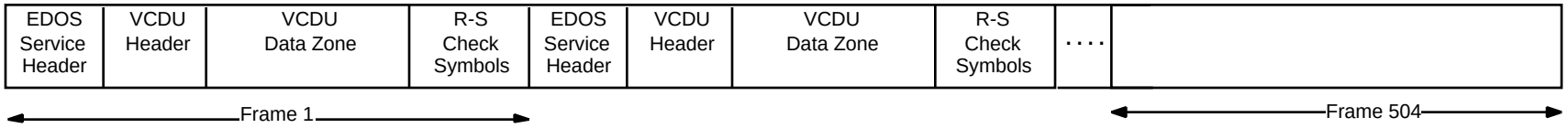


High Rate Return Link Prototype

Functional Overview



PCWG (Physical Channel Work Group) consists of 504 Frames

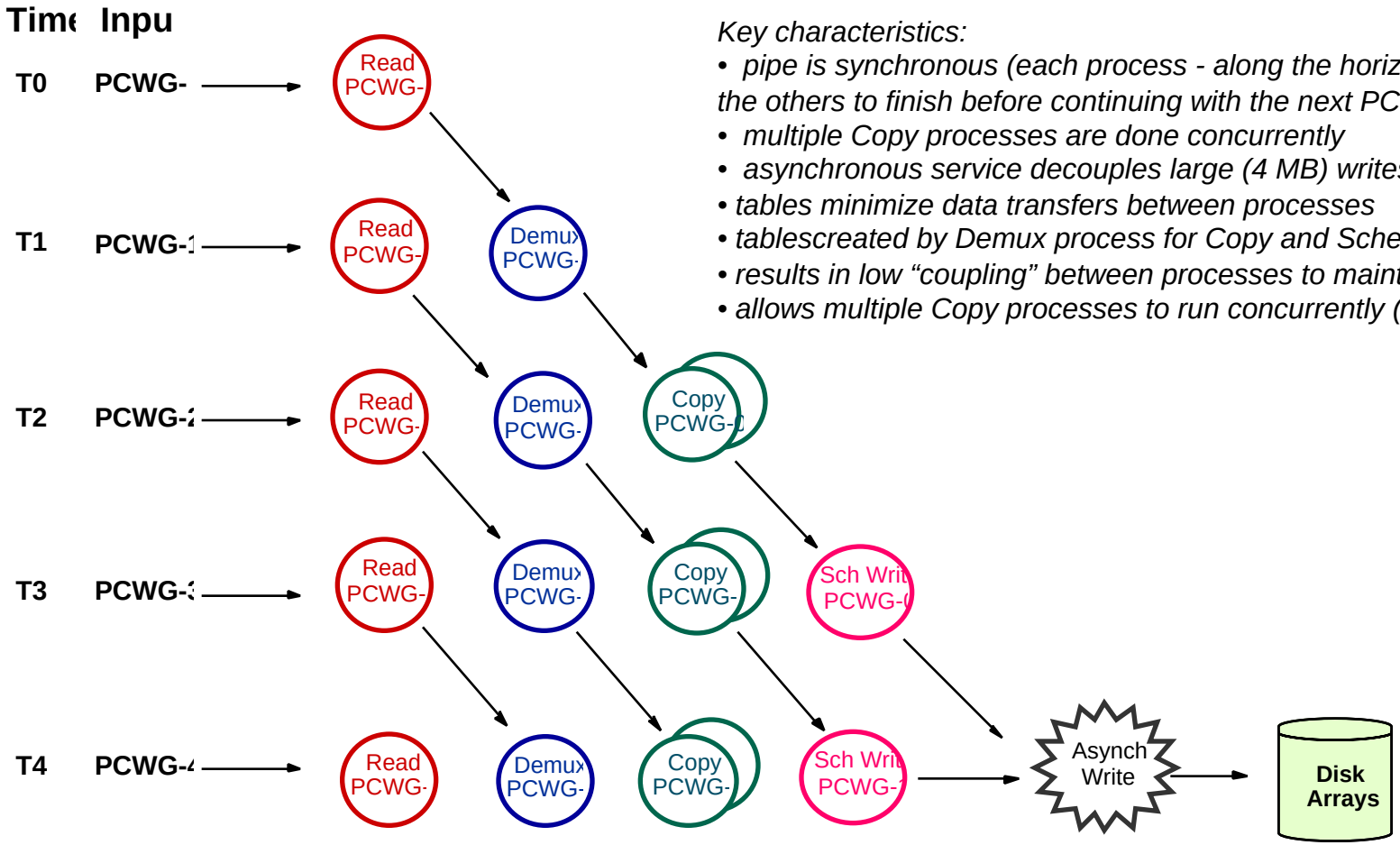


HRRL Service Processor Software Architecture

- Designed for a Symmetric Multiprocessor (SMP) - single computer with multiple CPUs that execute concurrently
  - EDOS SMP is an SGI Challenge with 8 CPUs (prototype uses 5 CPUs)
- HRRL functions were decomposed into 4 “processes” that simultaneously perform their task (*pipeline*)
  - Read - obtains the telemetry data from HiPPI and stores in memory
  - Demux - (virtual sort) demultiplexes the data and creates instruction tables to identify and group the data by VCID and APID
  - Copy - (physical sort) uses the instruction table to read data from and copy data to memory; multiple Copy processes execute concurrently
  - Schedule Write - monitors the Copy processes and uses the instruction table to schedule a write when a memory buffer is full
- Service routine performs asynchronous output of data to the

High Rate Return Link Prototype

HRRL Service Processor Pipeline Processing

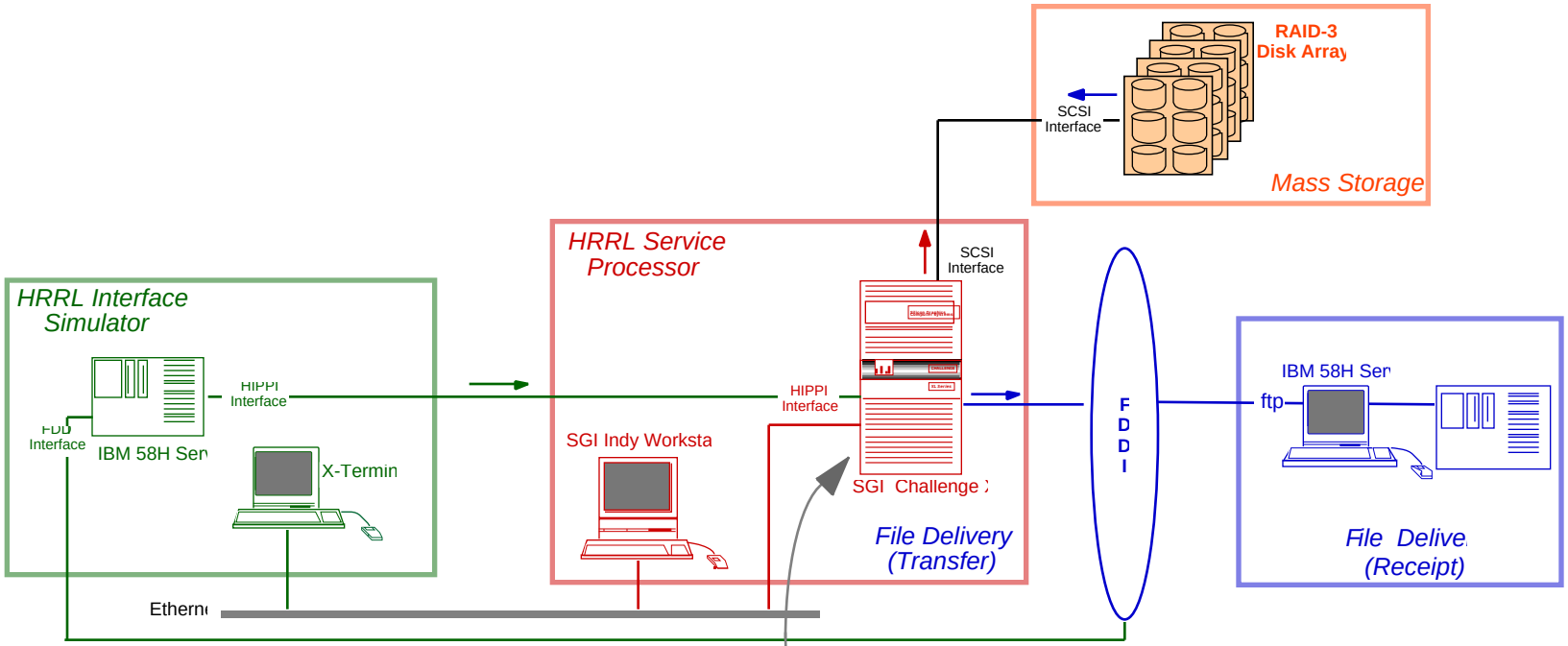


Key characteristics:

- *pipe is synchronous (each process - along the horizontal - waits the others to finish before continuing with the next PCWG)*
- *multiple Copy processes are done concurrently*
- *asynchronous service decouples large (4 MB) writes from the p*
- *tables minimize data transfers between processes*
- *tablescreated by Demux process for Copy and Schedule Write p*
- *results in low "coupling" between processes to maintain efficienc*
- *allows multiple Copy processes to run concurrently (table is split*

High Rate Return Link Prototype

Hardware Architecture



- *(8) 200 MHz R4400 CPUs (expandable to 36 processors)*
- *Data Cache: 16 KB (per CPU)*
- *Instruction Cache: 16 KB (per CPU)*
- *Secondary Unified Instruction/Data Cache: 4MB (Per CPU)*
- *Main Memory: 256 MB, 2-way interleaved*
- *Disks: (4) RAID-3 Disk Arrays over (4) SCSI (F/W) Controllers*

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HRRL Prototyping Results

- Virtual Channel Service
  - EDOS requirement: 150 Mbps (18,400 frames per second)
  - maximum achieved rate: 377 Mbps (45,000 frames per second)
- Path Service
  - EDOS requirement:
    - 40,000 packets per second (400 byte packets) @ 150 Mbps
  - maximum achieved rates:
    - 172,000 packets per second (100 byte packets) @ 154 Mbps
    - 206,000 packets per second (80 byte packets) @ 148 Mbps
    - 104,000 packets per second (400 byte packets) if input rate rate is unconstrained (375 Mbps)

HRRL Prototyping Results (Continued)

- Processing rates sensitivities
  - PCWG size
    - the bigger the PCWG, the less computer load incurred per transfer
    - selection of the PCWG size was a direct output of prototyping and the generation of the Harris RLFC ICD
      - recommended PCWG size is 0.5 MB - consistent with ending on a full frame
  - Packet and VCDU size - AM-1 specs
    - small packet and small VCDUs require similar processing resources
    - testing using a variety of packet sizes (including AM-1 data specs) shows overall computer load increases as packet size decreases